

HEF4049B

Hex inverting buffers

Rev. 9 — 18 November 2011

Product data sheet

1. General description

The HEF4049B provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in [Table 3](#).

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Accepts input voltages in excess of the supply voltage
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- LOCMOS (Local Oxidation CMOS) to DTL/TTL converter
- HIGH sink current for driving two TTL loads
- HIGH-to-LOW level logic conversion

4. Ordering information

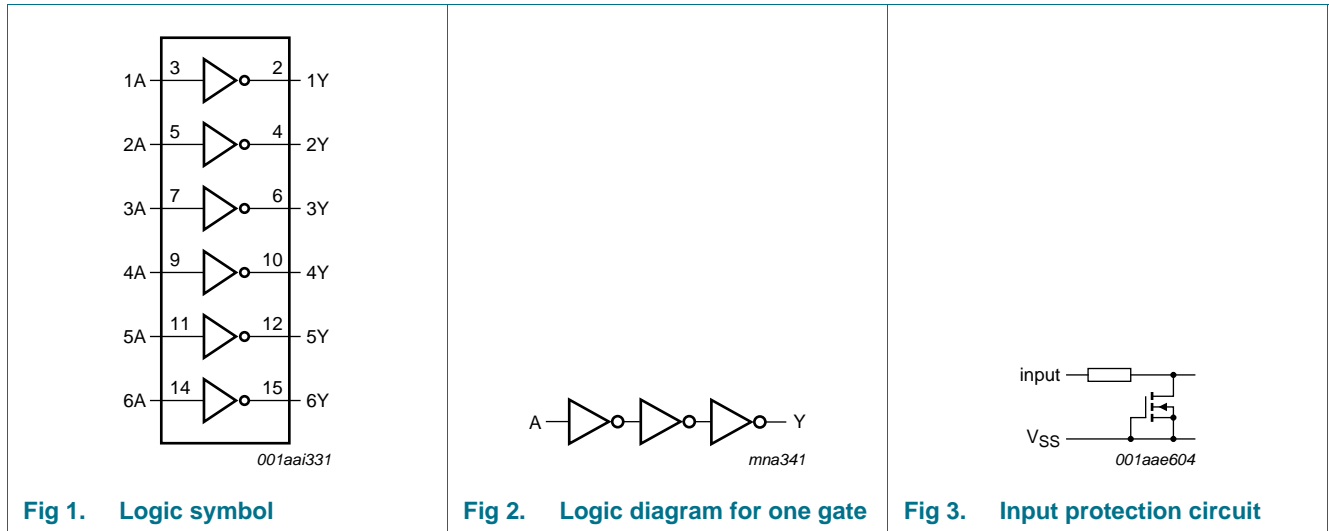
Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| HEF4049BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| HEF4049BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

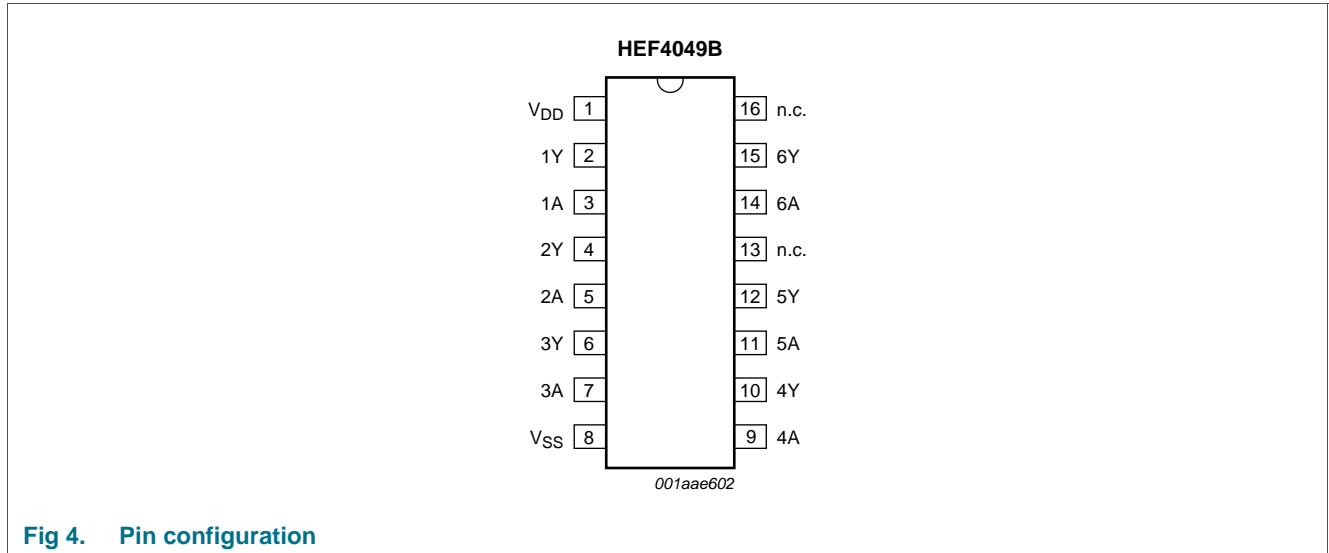


5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|---------------------|----------------|
| V _{DD} | 1 | supply voltage |
| 1Y to 6Y | 2, 4, 6, 10, 12, 15 | output |

Table 2. Pin description ...continued

| Symbol | Pin | Description |
|-----------------|--------------------|-----------------------|
| 1A to 6A | 3, 5, 7, 9, 11, 14 | input |
| V _{SS} | 8 | ground supply voltage |
| n.c. | 13, 16 | not connected |

7. Functional description

Table 3. Guaranteed fan-out

| Driven element | Guaranteed fan-out |
|----------------|--------------------|
| Standard TTL | 2 |
| 74 LS | 9 |
| 74 L | 16 |

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|-------|-----------------------|------|
| V _{DD} | supply voltage | | -0.5 | +18 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{DD} + 0.5 V | - | ±10 | mA |
| V _I | input voltage | | -0.5 | V _{DD} + 0.5 | V |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{DD} + 0.5 V | - | ±10 | mA |
| I _{I/O} | input/output current | | - | ±10 | mA |
| I _{DD} | supply current | | - | 50 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _{amb} | ambient temperature | | -40 | +85 | °C |
| P _{tot} | total power dissipation | T _{amb} -40 °C to +85 °C | | | |
| | | DIP16 package | [1] - | 750 | mW |
| | | SO16 package | [2] - | 500 | mW |
| P | power dissipation | per output | - | 100 | mW |

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------|-------------|-----|-----|-----------------|------|
| V _{DD} | supply voltage | | 3 | - | 15 | V |
| V _I | input voltage | | 0 | - | V _{DD} | V |
| T _{amb} | ambient temperature | in free air | -40 | - | +85 | °C |

Table 5. Recommended operating conditions ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|------------------------|-----|-----|------|-----------------|
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD} = 5\text{ V}$ | - | - | 3.75 | $\mu\text{s/V}$ |
| | | $V_{DD} = 10\text{ V}$ | - | - | 0.5 | $\mu\text{s/V}$ |
| | | $V_{DD} = 15\text{ V}$ | - | - | 0.08 | $\mu\text{s/V}$ |

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{\text{amb}} = -40\text{ }^\circ\text{C}$ | | $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ | | $T_{\text{amb}} = 85\text{ }^\circ\text{C}$ | | Unit |
|----------|---------------------------|--------------------------------|----------|--|-----------|---|-----------|---|-----------|---------------|
| | | | | Min | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| V_{IL} | LOW-level input voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| V_{OH} | HIGH-level output voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| V_{OL} | LOW-level output voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| I_{OH} | HIGH-level output current | $V_O = 2.5\text{ V}$ | 5 V | - | -1.7 | - | -1.4 | - | -1.1 | mA |
| | | $V_O = 4.6\text{ V}$ | 5 V | - | -0.52 | - | -0.44 | - | -0.36 | mA |
| | | $V_O = 9.5\text{ V}$ | 10 V | - | -1.3 | - | -1.1 | - | -0.9 | mA |
| | | $V_O = 13.5\text{ V}$ | 15 V | - | -3.6 | - | -3.0 | - | -2.4 | mA |
| I_{OL} | LOW-level output current | $V_O = 0.4\text{ V}$ | 4.75 V | 3.5 | - | 2.9 | - | 2.3 | - | mA |
| | | $V_O = 0.5\text{ V}$ | 10 V | 12.0 | - | 10.0 | - | 8.0 | - | mA |
| | | $V_O = 1.5\text{ V}$ | 15 V | 24.0 | - | 20.0 | - | 16.0 | - | mA |
| I_I | input leakage current | $V_{DD} = 15\text{ V}$ | 15 V | - | ± 0.3 | - | ± 0.3 | - | ± 1.0 | μA |
| I_{DD} | supply current | $I_O = 0\text{ A}$ | 5 V | - | 4.0 | - | 4.0 | - | 30 | μA |
| | | | 10 V | - | 8.0 | - | 8.0 | - | 60 | μA |
| | | | 15 V | - | 16.0 | - | 16.0 | - | 120 | μA |
| C_I | input capacitance | | | - | - | - | 7.5 | - | - | pF |

11. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $C_L = 50\text{ pF}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | Extrapolation formula | Min | Typ | Max | Unit |
|-----------|------------------------------------|---|----------|---|-----|-----|-----|------|
| t_{PHL} | HIGH to LOW propagation delay | nA to nY; see Figure 5 | 5 V | [1] $26\text{ ns} + (0.18\text{ ns/pF})C_L$ | - | 35 | 70 | ns |
| | | | 10 V | $11\text{ ns} + (0.08\text{ ns/pF})C_L$ | - | 15 | 30 | ns |
| | | | 15 V | $9\text{ ns} + (0.05\text{ ns/pF})C_L$ | - | 12 | 25 | ns |
| t_{PLH} | LOW to HIGH propagation delay | nA to nY; see Figure 5 | 5 V | [1] $23\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 50 | 100 | ns |
| | | | 10 V | $14\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 25 | 50 | ns |
| | | | 15 V | $12\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 20 | 40 | ns |
| t_{THL} | HIGH to LOW output transition time | see Figure 5 | 5 V | [1] $3\text{ ns} + (0.35\text{ ns/pF})C_L$ | - | 20 | 40 | ns |
| | | | 10 V | $3\text{ ns} + (0.14\text{ ns/pF})C_L$ | - | 10 | 20 | ns |
| | | | 15 V | $2\text{ ns} + (0.09\text{ ns/pF})C_L$ | - | 7 | 14 | ns |
| t_{TLH} | LOW to HIGH output transition time | see Figure 5 | 5 V | [1] $10\text{ ns} + (1.00\text{ ns/pF})C_L$ | - | 60 | 120 | ns |
| | | | 10 V | $9\text{ ns} + (0.42\text{ ns/pF})C_L$ | - | 30 | 60 | ns |
| | | | 15 V | $6\text{ ns} + (0.28\text{ ns/pF})C_L$ | - | 20 | 40 | ns |

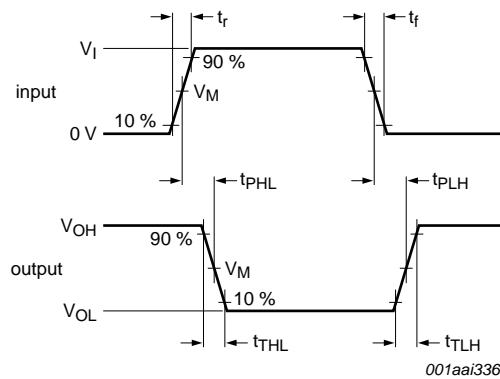
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ °C}$.

| Symbol | Parameter | V_{DD} | Typical formula for P_D (μW) | where: |
|--------|---------------------------|----------|---|---|
| P_D | dynamic power dissipation | 5 V | $P_D = 2500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f_i = input frequency in MHz; |
| | | 10 V | $P_D = 11000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f_o = output frequency in MHz; |
| | | 15 V | $P_D = 35000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs. |

12. Waveforms

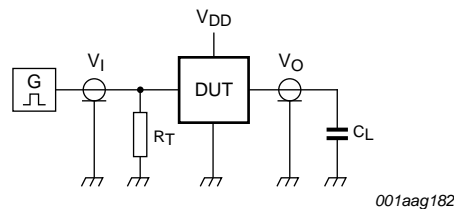


Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Input (nA) to output (nY) propagation delays and transition times

Table 9. Measurement points

| Input | | Output | | |
|-------------|-----------------|-------------|-------------|-------------|
| V_M | V_I | V_M | V_X | V_Y |
| $0.5V_{DD}$ | 0 V to V_{DD} | $0.5V_{DD}$ | $0.1V_{DD}$ | $0.9V_{DD}$ |



Test data is given in [Table 10](#).
 Definitions for test circuit:
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 6. Load circuitry for switching times

Table 10. Test data

| Supply voltage | Input | | | Load |
|----------------|----------|----------|--------------|-------|
| | V_I | V_M | t_r, t_f | C_L |
| 5 V to 15 V | V_{DD} | $0.5V_I$ | ≤ 20 ns | 50 pF |

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

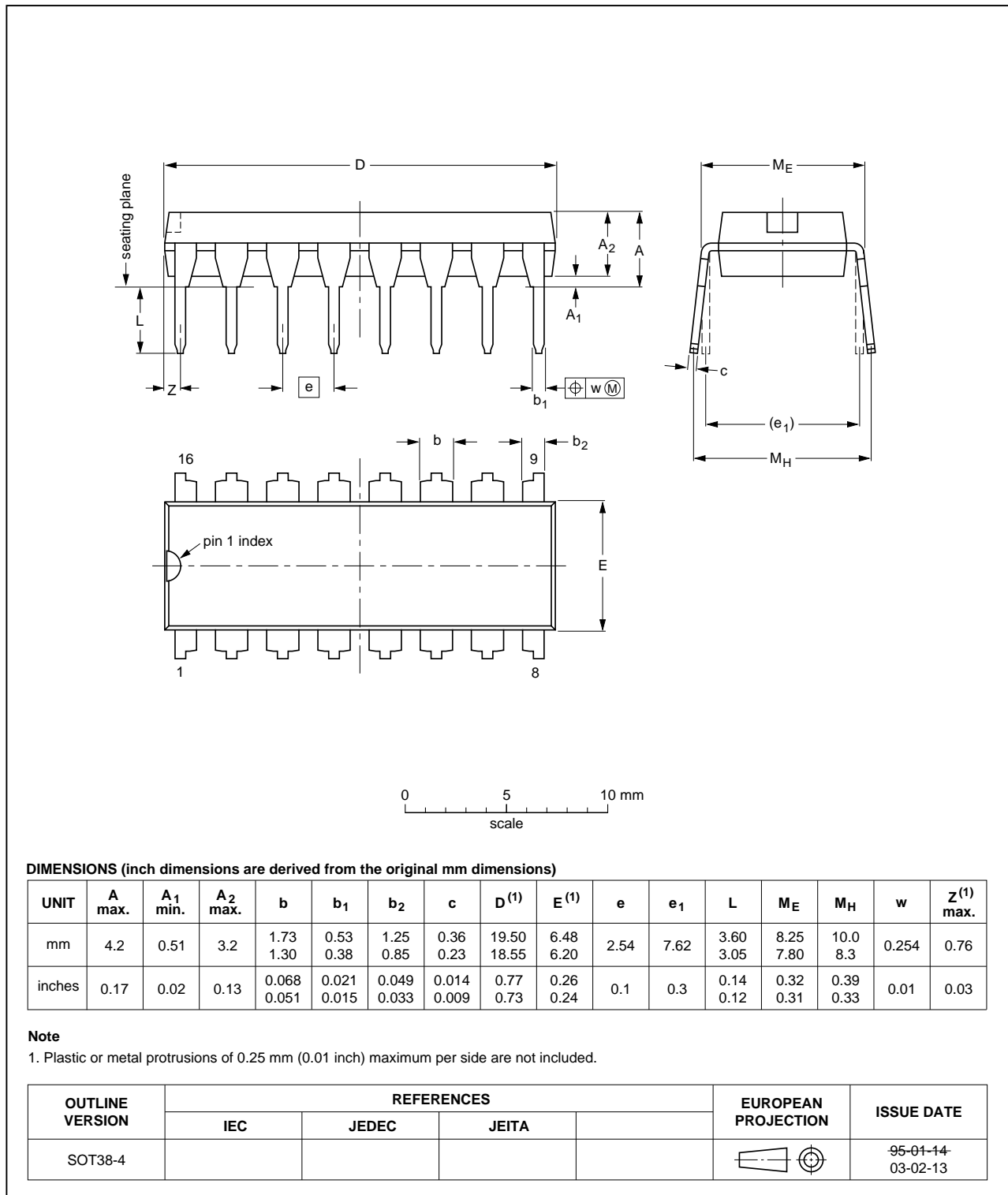


Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

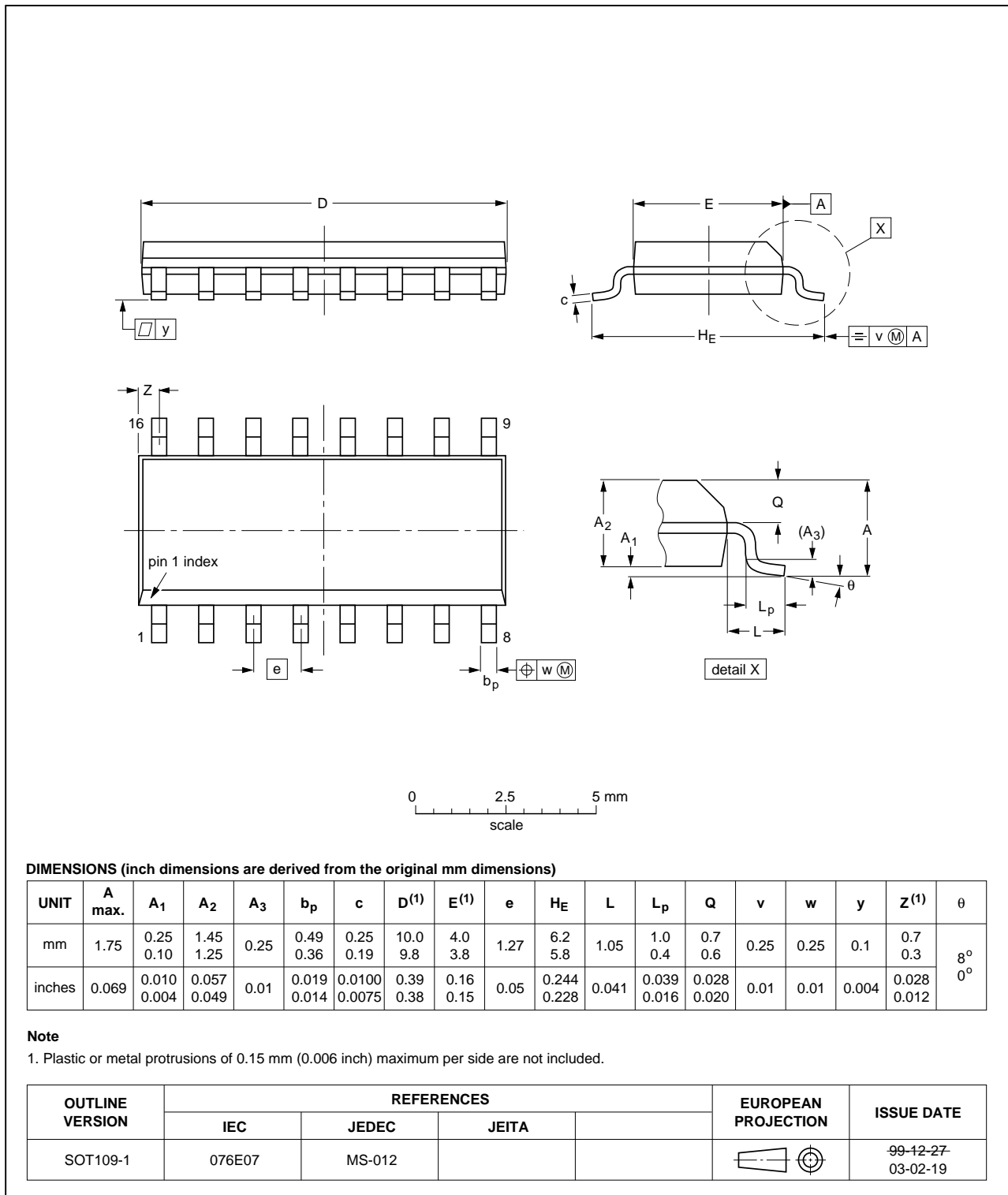


Fig 8. Package outline SOT109-1 (SO16)

14. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|-----------------------------|
| DTL | Diode Transistor Logic |
| DUT | Device Under Test |
| LOC MOS | Local Oxidation CMOS |
| TTL | Transistor Transistor Logic |

15. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--|-----------------------|---------------|------------------|
| HEF4049B v.9 | 20111118 | Product data sheet | - | HEF4049B v.8 |
| Modifications: | <ul style="list-style-type: none"> • Table 6: I_{OH} minimum values changed to maximum • Table 11: Added DUT | | | |
| HEF4049B v.8 | 20091202 | Product data sheet | - | HEF4049B v.7 |
| HEF4049B v.7 | 20090721 | Product data sheet | - | HEF4049B v.6 |
| HEF4049B v.6 | 20090325 | Product data sheet | - | HEF4049B v.5 |
| HEF4049B v.5 | 20081111 | Product data sheet | - | HEF4049B v.4 |
| HEF4049B v.4 | 20080704 | Product data sheet | - | HEF4049B_CNV v.3 |
| HEF4049B_CNV v.3 | 19950101 | Product specification | - | HEF4049B_CNV v.2 |
| HEF4049B_CNV v.2 | 19950101 | Product specification | - | - |

16. Legal information

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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